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(54) Fully planarized dual damascene metallization using copper line interconnect and selective CVD aluminium plug

(57) The present invention generally provides a metallization process for forming a highly integrated interconnect. More particularly, the present invention provides a dual damascene interconnect module that incorporates selective chemical vapor deposition aluminium (CVD Al) via fill with a metal wire, preferably copper, formed within a barrier layer. The invention provides the advantages of having copper wires with lower resistivity (greater conductivity) and greater electromigration resistance than aluminium, a barrier layer between the copper wire and the surrounding dielectric material, void-free, sub-half micron selective CVD Al via plugs, and a reduced number of process steps to achieve such integration.

FIG. 1A

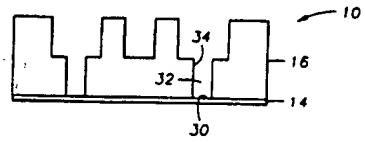


FIG. 1B

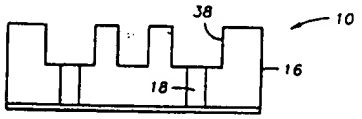


FIG. 1C

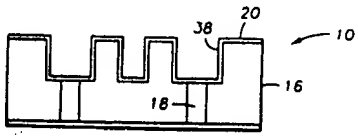


FIG. 1D

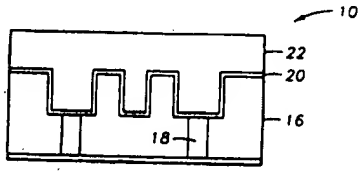
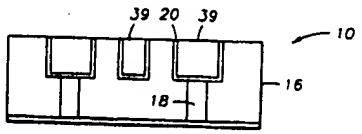


FIG. 1E



EP 0 851 483 A2

Description

The present invention relates to a metallization method for manufacturing semiconductor devices. More particularly, the present invention relates to fully planarized dual damascene metallization using a copper line interconnect and a selective CVD metal via plug.

Sub-half micron multilevel metallization is one of the key technologies for the next generation of very large scale integration (VLSI). The multilevel interconnects that lie at the heart of this technology require planarization of interconnect features formed in high aspect ratio apertures, including contacts, vias, lines or other features. Reliable formation of these interconnect features is very important to the success of VLSI and to the continued effort to increase circuit density and quality on individual substrates and die.

As circuit densities increase, the widths of vias, contacts and other features, as well as the dielectric materials between them, must decrease. Therefore, there is a great amount of ongoing effort being directed at the formation of smaller and smaller void-free features. One such method involves selective chemical vapor deposition (CVD) of material only on exposed nucleation surfaces as provided on the substrate surface. Selective CVD involves the deposition of a film layer upon contact of a component of the chemical vapor with a conductive substrate. The component nucleates on such substrate creating a metal surface on which further deposition proceeds.

Selective CVD metal deposition is based on the fact that the decomposition of a CVD metal precursor gas usually requires a source of electrons from a conductive nucleation film. In accordance with a conventional selective CVD metal deposition process, the metal should grow in the bottom of an aperture where either a metal film or doped silicon or metal silicide from the underlying conductive layer has been exposed, but should not grow on dielectric surfaces such as the field and aperture walls. The underlying metal films or doped silicon are electrically conductive, unlike the dielectric field and aperture walls, and supply the electrons needed for decomposition of the metal precursor gas and the resulting deposition of the metal. The result obtained through selective deposition is an epitaxial "bottom-up" growth of CVD metal in the apertures capable of filling very small dimension (<0.25 μm), high aspect ratio (>5:1) via or contact openings.

Elemental aluminum (Al) and its alloys have been the traditional metals used to form lines and plugs in semiconductor processing because of aluminum's low resistivity, superior adhesion to silicon dioxide (SiO_2), ease of patterning, and high purity. Furthermore, aluminum precursor gases are available which facilitate the selective CVD process described above. However, aluminum has higher resistivity and problems with electromigration. Electromigration is a phenomenon that occurs in a metal circuit while the circuit is in operation, as opposed to a failure occurring during fabrication. Electromigration is caused by the diffusion of the metal in the electric field set up in the circuit. The metal gets transported from one end to the other afier hours of operation and eventually separates completely, causing an opening in the circuit. This problem is sometimes overcome by Cu doping and texture improvement. However, electromigration is a problem that gets worse as the level of integration increases.

Copper and its alloys, on the other hand, have even lower resistivities than aluminum and significantly higher electromigration resistance. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increase device speed. However, the primary problems with integrating copper metal into multilevel metallization systems are (1) the difficulty of patterning the metal using etching techniques, and (2) filling small vias using PVD and lack of CVD process. For devices of submicron minimum feature size, wet etch techniques for copper patterning have not been acceptable due to liquid surface tension, isotropic etch profile, and difficulty in overetch control and reliable no dry etch process is available.

Several methods have been proposed for producing patterned copper interconnects, including selective electroless plating, selective chemical vapor deposition, high temperature reactive ion etching and lift off processing. Electroless plating requires that the floor of an interconnect be seeded to make the floor conductive. The conductive floor can then be charged to attract copper from a solution or bath.

Selective chemical vapor deposition typically involves the decomposition of a metal precursor gas on an electrically conducting surface. However, a reliable process for selective CVD copper is not available.

High temperature reactive ion etching (RIE), or sputter etching, has also been used to pattern a copper layer. Furthermore, the RIE can be used in conjunction with lift off processing in which excess metal is lifted of the structure by a release layer to leave a planar surface having a copper feature formed therein.

Yet another technique for metal wiring of copper comprises the patterning and etching of a trough and/or contact within a thick layer of insulating material, such as SiO_2. Thereafter, a thin layer of a barrier metal, such as Ti, TiW or TiN, may be provided on top of the insulating layer and within the trough and/or contact to act as a diffusion barrier to prevent inter-diffusion of the metal to be subsequently deposited into the silicon, and between such metal and oxide. After barrier metal deposition, a layer of copper is deposited to completely fill the trench.

Despite the availability of these techniques, there remains a need for a copper metallization process for fabricating interconnects at high levels of integration. Such highly integrated interconnects must provide void-free vias, particularly in high aspect ratio, sub-quarter micron wide apertures for forming contacts and vias. Furthermore, there is a need for

a process providing a circuit with higher electrical conductivity and improved electromigration resistance. It would be desirable to have a simple process requiring fewer processing steps to form metal plugs in the vias and wires in the trenches. It would be further desirable if the process could achieve all this without the use of metal etch techniques.

The present invention provides a method for forming a dual damascene interconnect in a dielectric layer having dual damascene via and wire definitions, wherein the via has a floor exposing a deposition enhancing material. The method includes selective chemical vapor deposition of a conductive metal, preferably aluminum, on the deposition enhancing material of the via floor to form a plug in the via. A barrier layer is then deposited over the exposed surfaces of the plug and wire definition. The wire definition is then filled by depositing a conductive metal, preferably copper, over the barrier layer. Finally, the conductive metal, the barrier and the dielectric layers are planarized, such as by chemical mechanical polishing, to define a conductive wire.

Another aspect of the invention provides a method of forming a dual damascene interconnect module over a deposition enhancing material. This method further includes the steps of forming a dielectric layer over the deposition enhancing material and then etching the dielectric layer to form a dual damascene via and wire definition, wherein the via has a floor exposing a deposition enhancing material. Where a substrate does not already have a layer of a deposition enhancing material, this layer may be provided prior to forming the dielectric layer. Furthermore, a multilevel metal interconnect may be formed in accordance with the invention by depositing a subsequent barrier layer of a deposition enhancing material over the planarized layers. A dielectric layer is subsequently formed and filled by repeating the steps described above.

So that the manner in which the above recited features, advantages and objects of the present invention are attained can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefor not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

Figures 1A through 1E show a dual damascene via and wire definition and steps for providing a metal interconnect in accordance with a first embodiment of the present invention.

Figures 2A through 2F show a dual damascene via and wire definition and steps for providing a metal interconnect in accordance with a second embodiment of the present invention.

Figure 3 is an integrated processing system configured for sequential metallization in accordance with the present invention.

The present invention generally provides an in-situ metallization process providing an interconnect in a highly integrated structure which has a reduced interconnect resistance and improved electromigration performance. More particularly, the present invention provides a dual damascene interconnect that incorporates selective chemical vapor deposition (CVD) metal fill of the via with a copper wire formed on a barrier layer. The present invention provides the advantages of having (1) copper wires with lower resistivity (greater conductivity) and greater electromigration resistance than aluminum, (2) a barrier layer between the copper wire and the surrounding dielectric material, (3) void-free, sub-half micron selective CVD metal via plugs, and (4) a reduced number of process steps.

For clarity, the present invention will be described below with reference to a selective CVD Al process for forming via plugs and a PVD Cu process for forming wires. However, other selective CVD metal processes and other PVD metal processes, such as PVD Al/Cu, may be used to accomplish the advantages of the present invention.

In one aspect of the invention, a method is provided for forming dual damascene interconnects having lower resistivity and greater electromigration resistance. The method utilizes a dual damascene via and wire definition etched into a dielectric layer. A sub-half micron via is filled without voids by selective CVD Al. The wire definitions are then given a barrier layer and filled with copper (Cu) using physical vapor deposition (PVD) techniques. The wires are completed by planarizing the structure.

In another aspect of the invention, a method is provided as described above with the additional step of depositing a warm PVD Al layer over the CVD Al plug and the exposed dielectric layers prior to forming the barrier layer. The warm PVD Al layer is deposited at a temperature greater than about 150°C and preferably greater than about 250°C. Warm PVD Al is desirable to provide a planarized metal film where a loss of selectivity in the CVD Al step creates nodules on the dielectric surface. These nodules are incorporated into a thin planarized metal layer to assure that the subsequently deposited barrier layer will be uniformly deposited with no void or gaps through which the copper can diffuse.

To form an IC structure in accordance with the present invention, a dielectric layer is formed by conventional techniques over a deposition enhancing material formed on a substrate. The dielectric layer may be as thick as about twice the thickness of a single metallization layer since a dual damascene via and wire definition will be etched therethrough. Any dielectric material, whether presently known or yet to be discovered, may be used and is within the scope of the present invention. The dielectric layer may be deposited on any suitable deposition enhancing material, but the preferred deposition enhancing materials include conductive metals and doped silicon.

Referring to Figures 1A through 1E, a cross-sectional diagram of a layered structure 10 is shown including a dielectric layer 16 formed over a deposition enhancing layer 14, preferably an electrically conducting member or layer. The

deposition enhancing layer 14 may take the form of a doped silicon substrate or it may be a first or subsequent conducting layer formed on a substrate. The dielectric layer 16 is formed over the deposition enhancing layer 14 in accordance with procedures known in the art to form a part of the overall integrated circuit.

Once deposited, the dielectric layer is etched to form a dual damascene via and wire, wherein the via has a floor 30 exposing a small portion of the deposition enhancing material 14. Etching of the dielectric layer 16 may be accomplished with any dielectric etching process, including plasma etching. Specific techniques for etching silicon dioxide and organic materials may include such compounds as buffered hydrofluoric acid and acetone or EKC, respectively. However, patterning may be accomplished using any method known in the art.

Referring to Figure 1A, a cross-sectional diagram of dual damascene via and wire definition 32 formed in the dielectric layer 16 is shown. The definition 32, formed according to the present invention, is generally intended to facilitate the deposition of a conductive interconnect that will provide an electrical connection with an underlying conductive member. The definition 32 provides via walls 34 and a floor 30 exposing at least a portion of the deposition enhancing material 14. The deposition enhancing material 14 may be a layer, wire or device comprising a metal, doped silicon or other conductive material. In particular, the deposition enhancing material may be provided by a barrier layer of a metal selected from the group consisting of aluminum, aluminum oxides, titanium, titanium nitride, tantalum, tantalum nitride and doped silicon. The presence of a conductive via floor is exploited according to the present invention to provide a selective CVD metal process to fill the via or plug. The preferred metal for selective CVD processing is aluminum. For example, a CVD Al film can be formed by the decomposition reaction of dimethyl aluminum hydride ("DMAH"). This particular reaction occurs much more rapidly when the reactants come in contact with a deposition enhancing material that is an electron donor, such as the surface of an electrically conductive material. Therefore, it is possible to achieve a certain measure of control or selectivity over where and how the CVD Al is deposited by preparing a structure with some surfaces that are conductive and some surfaces that are non-conductive.

Referring to Figure 1B, a cross-sectional view of a void-free metal plug 18 formed in the via 32 is shown. Selective CVD Al provides epitaxial growth of a void-free, single crystal plug. Despite the relative selectivity of the CVD Al, small amounts of the CVD Al can also deposit on the surfaces of the non-conductive dielectric layer 16 to form nodules if the surface includes defects that can serve as nucleation sites.

While the CVD Al may be deposited under various conditions, a typical process involves substrate temperatures of between about 120°C and about 280°C and a deposition rate of between about 20 Å/sec and about 200 Å/sec,. and between about 300 Å/sec. and about 1000 Å/sec. for selective CVD. The CVD Al deposition may be performed at chamber pressures of between about 1 tort and about 80 torr, with the preferred chamber pressure being about 25 torr. The preferred deposition reaction for CVD Al involves the reaction of dimethyl aluminum hydride ("DMAH") with hydrogen gas (H_2) according to the following equation:

$$6(CH_3)_2Al - H + 3H_2 \dashrightarrow 6Al + 12CH_4$$

or

$$(CH_3)_2 Al - H \dashrightarrow Al + 2\ TMA\ (trimethyl\ aluminum) + H_2$$

The deposition within the via 32 to form a metal interconnect 18 is selective because the surface 30 of the underlying conductive layer 14 has been exposed to the CVD Al at the floor of the via 32. Therefore, the CVD Al is deposited from the floor 30 upward to fill the aperture 32 without any substantial CVD Al deposition on the via walls 34.

Furthermore, the via 32 comprises substantially non-conductive dielectric walls 34 and the conductive floor 30. As discussed above, substantially non-conducting materials, such as the dielectric walls 34 of the aperture, are not good electron donors and, therefore, do not provide good nucleation for decomposition of the CVD metal precursor. Rather, the CVD metal film begins to form on the via floor 30 because the exposed conducting member 14 forming the floor of the via 32 nucleates the decomposition. After an initial layer of the metal has been deposited on the via floor 30, subsequent deposition occurs more easily so that the metal grows from the via floor 30 upward or outward to fill the via 32.

Although defects on the dielectric wall 34 of the via 32 may cause the formation of scattered nodules within the aperture, these nodules typically do not block the aperture to cause voids therein because nodule formation occurs at a much slower rate than selective growth. The via is filled with metal from the floor upward before a nodule has a opportunity to grow across the via and form a void therein, even in a via having an aspect ratio as high as 5:1, because the conducting via floor 30 exposes a much larger surface area than typical defects. The endpoint of the selective deposition is determined by the deposition rate and duration.

Referring to Figure 1C, a barrier layer 20 is deposited over the aluminum plug 18 as well as the walls and floor of the wire definition 38. The barrier layer is preferably formed of titanium, titanium nitride, tantalum or tantalum nitride. The process used may be PVD or CVD. The barrier layer limits the diffusion of copper and dramatically increases the reliability of the aluminum plug 18. It is preferred that the barrier layer having a thickness between about 50 and about

400 Angstroms (A), most preferably about 200 A.

Referring to Figure 1D, copper 22 is physical vapor deposited over the barrier layer 20 to fill the wire definition 38 (see Figure 1C). In order to fill the wire definition, it will generally occur that the entire field of the structure will become covered with the PVD Cu.

Referring to Figure 1E, the top portion of the structure 10 is then planarized, preferably by chemical mechanical polishing (CMP). During the planarization process, portions of the copper 22, barrier material 20 and dielectric 16 are removed from the top of the structure leaving a fully planar surface with a conductive wire 39 formed therein.

In accordance with a second aspect of the invention, the method described above may further comprise the step of physical vapor depositing a thin layer of aluminum over the exposed surfaces of the plug and wire definition prior to forming the barrier layer. The purpose of the thin PVD Al layer is to smooth over any nodules formed on the surfaces of the wire definition so that the barrier layer will be uniform and continuous.

Referring to Figures 2A through 2F, the steps involved in this second aspect of the invention are set out. Figures 2A and 2B are the same as Figures 1A and 1B, respectively. Figure 2C shows the PVD Al layer 42 formed over the structure 40 from Figure 2B. The PVD Al provides a smooth layer that incorporates any nodules formed during the previous step of selective CVD Al. The preferred thickness for the PVD Al layer 42 is between about 100 Å and about 700 A. Figures 2D through 2F then detail the deposition of a barrier layer 20, deposition of a PVD Cu layer 22, and planarization of the structure 40 in a similar fashion as set out above in Figures 1C through 1E, respectively. Therefore, the second aspect of the invention is vastly similar to the process first described, but with the addition of an intermediate step of depositing a PVD Al layer 42 between the CVD Al plug 18 and the barrier layer 20.

In yet another aspect of the present invention, a method of forming a multilevel metal interconnect is provided. First, a layer of a deposition enhancing material is provided on a workpiece. A dielectric layer is then formed over the exposed layer of deposition enhancing material and etched to form a dual damascene via and wire definition, wherein the via has a floor exposing the deposition enhancing material. Selective chemical vapor deposition of aluminum (CVD Al) is performed to deposit aluminum on the deposition enhancing material of the via floor to form a plug in the via. At this stage, the interconnect may optionally receive a thin layer of PVD Al over the exposed surfaces of the plug and wire definition. This optional layer is helpful to smooth over aluminum nodules on dielectric surfaces caused by loss of selectivity, as described above.

Next, a first barrier layer is deposited over the aluminum plug and dielectric surfaces or, alternatively, over the optional PVD Al layer. PVD Cu is then deposited over the barrier layer to fill the wire definition. The copper, barrier, aluminum and dielectric layers that comprise the structure are planarized, preferably by CMP, to define a conductive wire. A second barrier layer, that can also function as a deposition enhancing material, is then deposited over the planarized layers. In this manner, the copper wire is enclosed by barrier layers to prevent diffusion of the copper and the a deposition enhancing layer is provided so that the process can be repeated any number of times to form a multilevel module. When the last barrier layer has been deposited over the last copper wire, it is preferred that a passivating layer be applied over the top.

The methods of the present invention is preferably carried out in an integrated cluster tool that has been prograined to process a substrate accordingly. Referring to Figure 3, a schematic diagram of an exemplary integrated cluster tool 60 is shown. A complete description of the cluster tools and its general operation are set out in commonly assigned U.S. Patent Application Serial No. 08/571,605, which is hereby incorporated by reference. The exact arrangement and combination of chambers may be altered for purposes of performing specific steps of a fabrication process.

In accordance with the present invention, the cluster tool 60 is preferably equipped with a microprocessor controller programmed to carry out the processing methods described above. In order to begin the process, a substrate must be introduced through a cassette loadlock 62. A robot 64 having a blade 67 transfers the substrate from the cassette loadlock 62 through the buffer chamber 68 to a degas wafer orientation chamber 70 and then to the preclean chamber 72.

The etched substrate is then taken by the robot into the selective CVD Al chamber 82 for void-free filling of the via to form a plug. Because certain nodules may be formed over the wire definition, it may be desirable to transfer the substrate to a warm PVD Al chamber 84 where deposition of warm aluminum planarizes the nodules.

The substrate is then transferred to chamber 86 to deposit a barrier layer over the plug and wire definition, preferably by physical vapor deposition. Copper is then deposited to fill the wire definition by physical vapor deposition. It is anticipated that the substrate may be processed or cooled in one or more chambers any number of times in any order to accomplish fabrication of the desired structure on the substrate. The substrate is then passed back through the transfer chamber 80, cooldown chamber 76 and buffer chamber 68 to the loadlock 62 so that the substrate can be removed. In order to complete the wire formation, the substrate is then sent to a chemical mechanical polishing apparatus (not shown) for planarization.

One staged-vacuum wafer processing system is disclosed in United States Patent No. 5,186,718, entitled "Staged-Vacuum Wafer Processing System and Method," Tepman et al., issued on February 16, 1993, which is hereby incorporated herein by reference.

While the foregoing is directed to the preferred embodiment of the present invention, other and ether embodiments

of the invention may be devised without departing from the basic scope thereof. The scope of the invention is determined by the claims which follow.

Claims

1. A method of forming a dual damascene interconnect in a dielectric layer having a dual damascene via and wire definition, wherein the via has a floor exposing a deposition enhancing material, the method comprising the steps of:

   (a) selectively chemical vapor depositing a first conductive metal on the deposition enhancing material of the via floor to form a plug in the via;
   (b) depositing a barrier layer over the exposed surfaces of the plug and dielectric wire definition;
   (c) depositing a second conductive metal over the barrier layer to fill the wire definition; and
   (d) planarizing the second conductive metal, barrier and dielectric layers to define a conductive wire.

2. A method as claimed in claim 1, wherein the second conductive metal is selected from copper, aluminium and mixtures thereof.

3. A method as claimed in claim 1 or claim 2, wherein the first conductive metal is aluminium.

4. A method of forming a dual damascene interconnect in a dielectric layer having a dual damascene via and wire definition, wherein the via has a floor exposing a deposition enhancing material, the method comprising the steps of:

   (a) selectively chemical vapor depositing aluminium on the deposition enhancing material of the via floor to form a plug in the via;
   (b) physical vapor depositing a thin layer of aluminium over the exposed surfaces of the plug and wire definition;
   (c) depositing a barrier layer over the aluminium layer;
   (d) depositing a conductive metal over the barrier layer to fill the wire definition; and
   (e) planarizing the conductive metal, barrier, aluminium and dielectric layers to define a conductive wire.

5. A method as claimed in claim 4, wherein the conductive metal is selected from copper, aluminum and mixtures thereof.

6. A method of forming a dual damascene interconnect module over a deposition enhancing material, the method comprising the steps of:

   (a) forming a dielectric layer over the deposition enhancing material;
   (b) etching the dielectric layer to form a dual damascene via and wire definition, wherein the via has a floor exposing a deposition enhancing material;
   (c) selectively chemical vapor depositing a conductive material on the deposition enhancing material of the via floor to form a plug in the via;
   (d) depositing a barrier layer over the exposed surfaces of the plug and wire definition;
   (e) physical vapor depositing copper over the barrier layer to fill the wire definition; and
   (f) planarizing the copper, barrier and dielectric layers to define a conductive wire.

7. A method as claimed in any one of claims 1 to 6, wherein the step of planarizing is performed by chemical mechanical polishing.

8. A method as claimed in claim 6, wherein the conductive material is aluminium.

9. A method of forming a dual damascene interconnect module, the method comprising the steps of:

   (a) forming a dielectric layer over a deposition enhancing material;
   (b) etching the dielectric layer to form a dual damascene via and wire definition, wherein the via has a floor exposing the deposition enhancing material;
   (c) selectively chemical vapor depositing aluminium on the deposition enhancing material of the via floor to form a plug in the via;
   (d) physical vapor depositing a thin layer of aluminium over the exposed surfaces of the plug and wire defini-

tion;

(e) depositing a barrier layer over the aluminium layer;
(f) physical vapor depositing copper over the barrier layer to fill the wire definition; and
(g) planarizing the upper surface of the structure to define a conductive wire.

10. A method as claimed in any one of claims 1 to 9, wherein the deposition steps are performed in an integrated processing system.

11. A method as claimed in any one of claims 1 to 10, wherein the barrier layer comprises a material selected from titanium, titanium nitride, tantalum, tantalum nitride, doped silicon, aluminium and aluminium oxides.

12. A method as claimed in any one of claims 6 to 11, wherein the deposition enhancing material is provided by a barrier layer of a material selected from titanium, titanium nitride, tantalum, tantalum nitride, doped silicon, aluminium and aluminium oxides.

13. A method of forming a multilevel metal interconnect, the method comprising the steps of:

(a) providing a layer of a deposition enhancing material on a workpiece;
(b) forming a dielectric layer over the exposed layer of deposition enhancing material;
(c) etching the dielectric layer to form a dual damascene via and wire definition, wherein the via has a floor exposing a deposition enhancing material;
(d) selectively chemical vapor depositing aluminium on the deposition enhancing material of the via floor to form a plug in the via;
(e) physical vapor depositing a thin layer of aluminium over the exposed surfaces of the plug and wire definition;
(f) depositing a first barrier layer over the aluminium layer;
(g) physical vapor depositing copper over the barrier layer to fill the wire definition;
(h) planarizing the copper, barrier, aluminium and dielectric layers to define a conductive wire;
(i) depositing a second barrier layer over the planarized layers, wherein the second barrier layer is a deposition enhancing material; and
(j) repeating steps (b) through (h).

14. A method as claimed in claim 13, further comprising the step of applying a passivating layer over the top planarized layer.

FIG. 1A

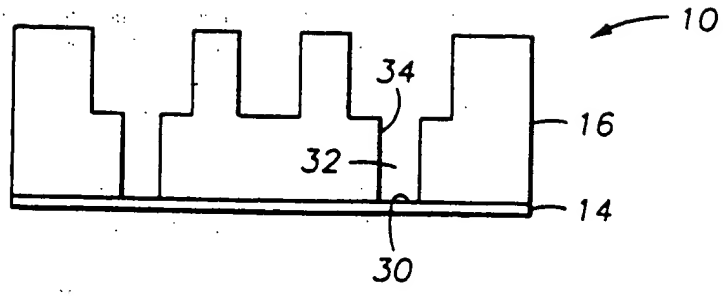


FIG. 1B

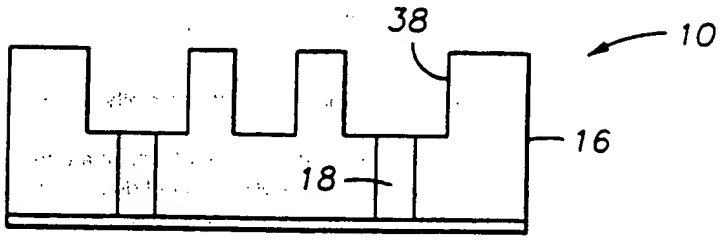


FIG. 1C

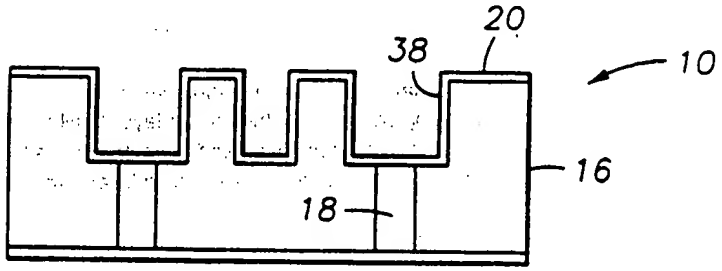


FIG. 1D

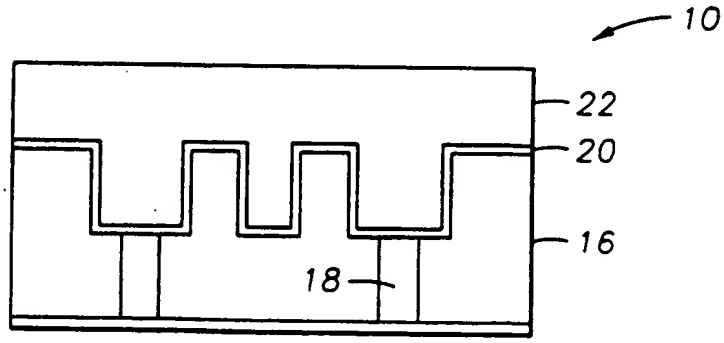


FIG. 1E

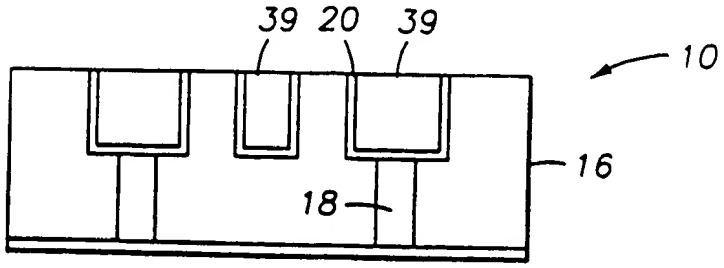


FIG. 2A

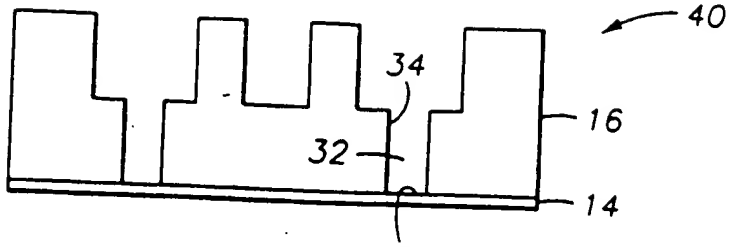


FIG. 2B

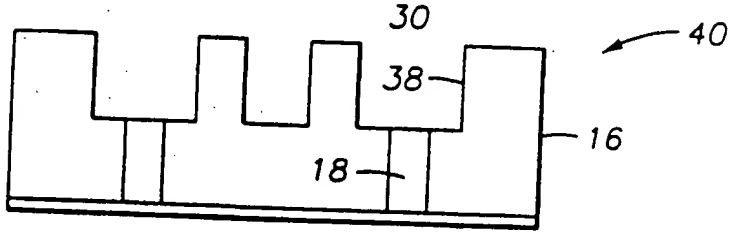


FIG. 2C

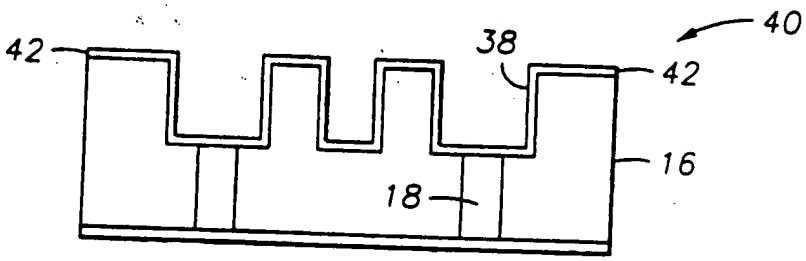


FIG. 2D

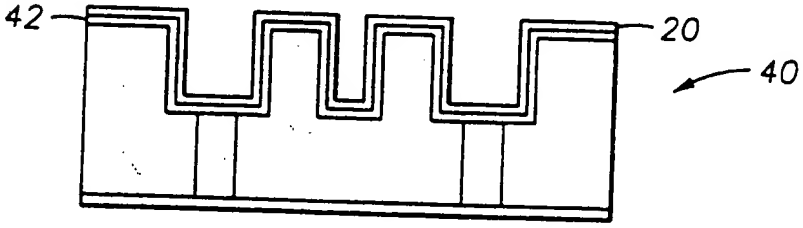


FIG. 2E

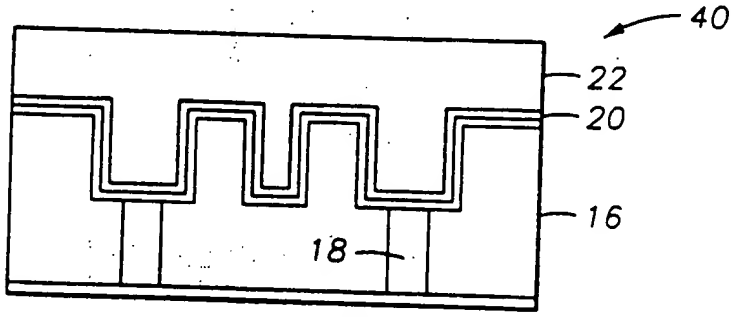
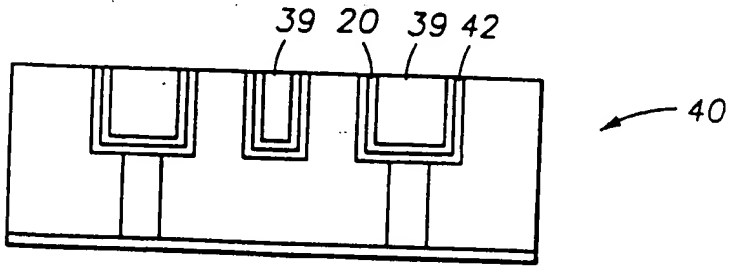


FIG. 2F



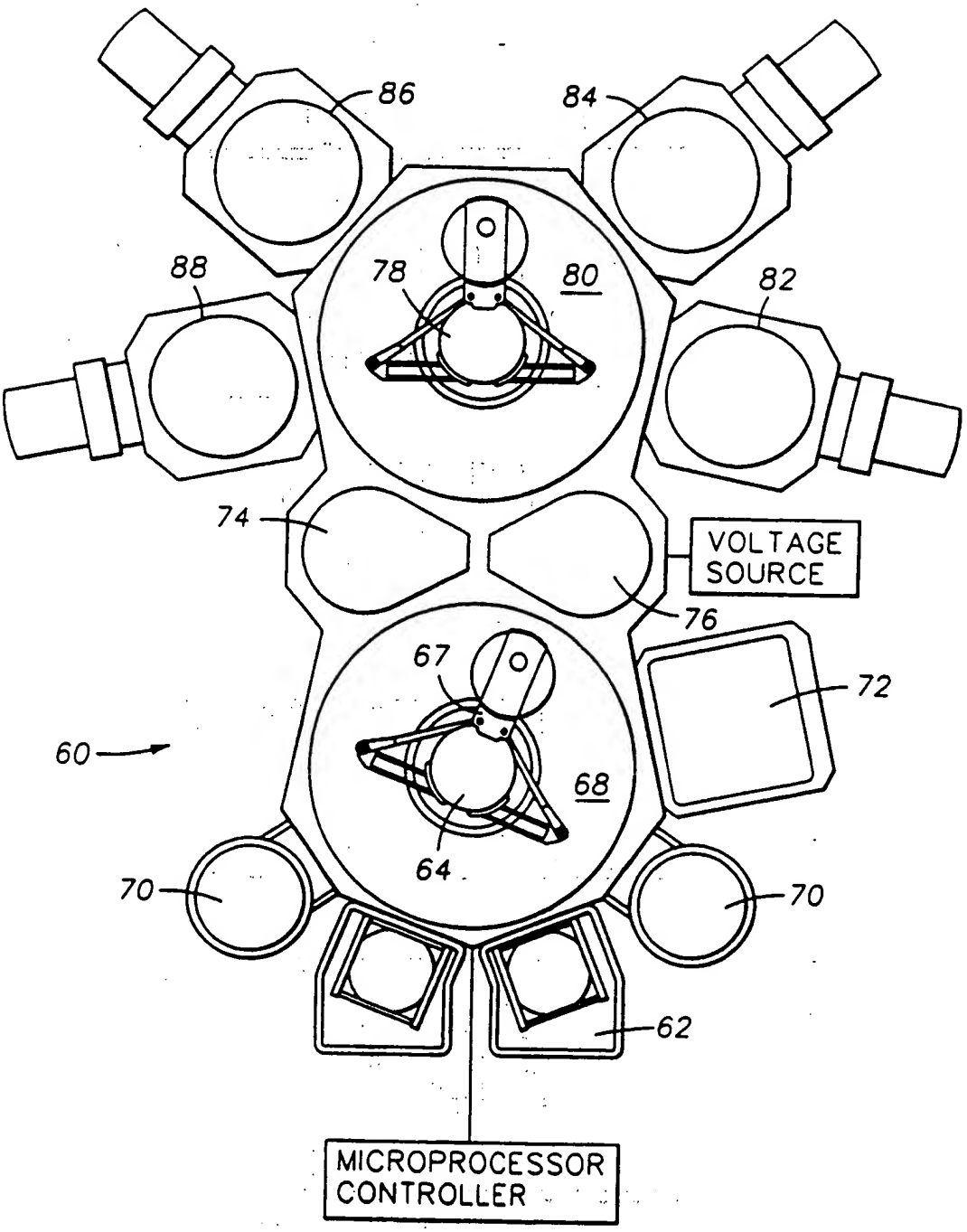

86
84
88
78
80
82
74
VOLTAGE SOURCE
76
67
72
60
68
64
70
70
62
MICROPROCESSOR CONTROLLER

FIG. 3

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

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(54) **Fully planarized dual damascene metallization using copper line interconnect and selective CVD aluminium plug**

(57) The present invention generally provides a metallization process for forming a highly integrated interconnect. More particularly, the present invention provides a dual damascene interconnect module that incorporates selective chemical vapor deposition aluminium (CVD Al) via fill with a metal wire, preferably copper, formed within a barrier layer. The invention provides the advantages of having copper wires with lower resistivity (greater conductivity) and greater electromigration resistance than aluminium, a barrier layer between the copper wire and the surrounding dielectric material, void-free, sub-half micron selective CVD Al via plugs, and a reduced number of process steps to achieve such integration.

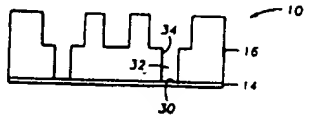

FIG. 1A

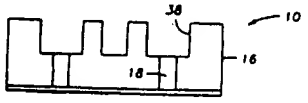

FIG. 1B

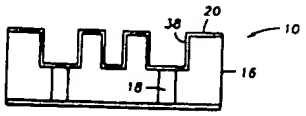

FIG. 1C

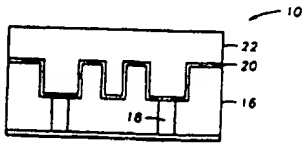

FIG. 1D

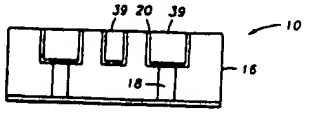

FIG. 1E

EP 0 851 483 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 31 0668

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 435 388 A (PHILIPS NV) 3 July 1991 (1991-07-03) * abstract; claims; figures * * column 2, line 28 - line 55 * * column 4, line 52 - column 6, line 55 * ---	1,4,6,7,9	H01L21/768 H01L21/285
A	EP 0 558 004 A (SIEMENS AG ;IBM (US)) 1 September 1993 (1993-09-01) * abstract; claims; figures * * column 4, line 5 - line 42 * * column 9, line 1 - column 10, line 52 * ---	1-9,13	
A	KAZUO TSUBOUCHI ET AL: "COMPLETE PLANARIZATION OF VIA HOLES WITH ALUMINUM BY SELECTIVE AND NONSELECTIVE CHEMICAL VAPOR DEPOSITION" APPLIED PHYSICS LETTERS, vol. 57, no. 12, 17 September 1990 (1990-09-17), pages 1221-1223, XP000163177 ISSN: 0003-6951 * the whole document * -----	4,9,13	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	25 August 1999	Hamdani, F

CATEGORY OF CITED DOCUMENTS

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EPO FORM 1503 03.82 (P04C01)

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25-08-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0435388 A	03-07-1991	US 4987099 A	22-01-1991
		DE 69025886 D	18-04-1996
		DE 69025886 T	02-10-1996
		JP 4030426 A	03-02-1992
EP 0558004 A	01-09-1993	US 5262354 A	16-11-1993
		AT 159615 T	15-11-1997
		CN 1076547 A,B	22-09-1993
		DE 69314679 D	27-11-1997
		DE 69314679 T	02-04-1998
		HK 1001601 A	26-06-1998
		JP 6084826 A	25-03-1994
		KR 9706973 B	01-05-1997

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82